

Azimuthal dependence of single-event and multiple-bit upsets in SRAM devices with anisotropic layout*

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Experimental evidence is presented showing obvious azimuthal dependence of single event upsets (SEU) and multiple-bit upset (MBU) patterns in radiation hardened by design (RHBD) and MBU-sensitive static random access memories (SRAMs), due to the anisotropic device layouts. Depending on the test devices, a discrepancy from 24.5% to 50% in the SEU cross sections of dual interlock cell (DICE) SRAMs is shown between two perpendicular ion azimuths under the same tilt angle. Significant angular dependence of the SEU data in this kind of design is also observed, which does not fit the inverse-cosine law in the effective LET method. Ion trajectory-oriented MBU patterns are identified, which is also affected by the topological distribution of sensitive volumes. Due to that the sensitive volumes are periodically isolated by the BL/BLB contacts along the Y-axis direction, double-bit upsets along the X-axis become the predominant configuration under normal incidence. Predominant triple-bit upset and quadruple-bit upset patterns are the same under different ion azimuths (L-shaped and square-shaped configurations, respectively). Those results suggest that traditional RPP/IRPP model should be promoted to consider the azimuthal and angular dependence of single event effects in certain designs. During earth-based evaluation of SEE sensitivity, worst case beam direction, i.e., the worst case response, should be revealed to avoid underestimation of the on-orbit error rate.

Keywords: Azimuth, Dual interlocked cell, Multiple-bit upset, Single event upset

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I. INTRODUCTION

Single event effects (SEEs) are becoming one of the critical reliability concerns for space-borne electronic devices, especially with technologies further downscaling [1, 2]. Thus, earth-based testing and modeling of single event performances to predict the on-orbit error rates are of significant importance to guarantee the reliability of integrated circuits (ICs) for space missions [3]. Rectangular parallelepiped (RPP) and integral rectangular parallelepiped (IRPP) models [4–7], whose efficacy has been verified by years of on-orbit performance data [8], have enjoyed almost 30 years of success and wide-spread use for error rate predictions in the space environment [9].

However, one of the inherent assumptions in the RPP/IRPP model is that charges deposited by single ions are collected in a single sensitive volume (SV), which may fail as applied to devices in which charge sharing effects between adjacent sensitive nodes cannot be neglected. For instance, multiple-bit upset (MBU) caused by single incident particles happens more frequently in advanced ICs due to the reduced distance between sensitive nodes. However, the RPP/IRPP model is incapable of predicting MBU accurately

and, hence, may underestimate the on-orbit error rates of MBU-sensitive devices. Additionally, radiation hardened by design (RHBD) techniques, such as dual interlocked cells (DICE) [10], triple modular redundancy (TMR), and active delay elements (ADE) [11], use redundant elements for the protection of circuits from single volume charge collection. Those structures will only be flipped by multiple volume charge collections and, hence, can be very sensitive to tilted and azimuthal ion incidence [12]. Consequently, instead of only using normally incident ions during earth-based heavy-ion testing, complete measurements, including angled ion strikes and azimuthal evaluation, should be performed to mimic the omnidirectional space radiation, find the worst-case beam direction, and avoid underestimation of the on-orbit performance of MBU-sensitive devices and devices hardened by redundant elements, especially for those with anisotropic layouts. Besides the published results on the azimuthal dependence of single event transients (SET) [3], single event upsets (SEU) [12–14], and MBU [15], more data should be collected to probe the inner mechanisms and contribute to the developments of accurate error rate prediction models based on or instead of the RPP/IRPP model.

In this work, MBU-sensitive and DICE static random access memories (SRAMs) were irradiated by heavy-ions with various tilt angles and azimuths to reveal the azimuthal dependence of single event responses and the underlying mechanisms. Obvious discrepancies in SEU cross sections under different ion azimuths are shown in the DICE-SRAM devices. Trajectory-oriented MBU patterns are identified in the

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TABLE 1. Description of DUTs including device type, manufacturer, organization, package, technology, and type

Device type	Manufacturer	Organization	Package	Technology	Type
B8R512K8b	Vendor A	4 Mb (512 kb \times 8)	TQFP	0.18 μ m CMOS	DICE
B8R256K32b	Vendor A	8 Mb (256 kb \times 32)	TQFP	0.18 μ m CMOS	DICE
IDT7164	IDT	64 kb (8 kb \times 8)	DIP	—	MBU-sensitive
IDT71256	IDT	256 kb (32 kb \times 8)	DIP	1.3 μ m 4T2R-NMOS	MBU-sensitive

anisotropic-layout devices, although the predominant triple-bit upset (TBU) and quadruple-bit upset (QBU) patterns are the same under different ion azimuths. The inner mechanisms are analyzed based on the device layout, which is obtained by a reverse-engineering technique.

The experimental setup is presented in Sec. II, including devices under test (DUTs), radiation source, test system, and MBU identification. Section III shows the experimental results and analysis. The implications for hardness assurance testing are discussed in Sec. IV.

II. EXPERIMENTAL SETUP

A. DUTs

In this work, two kinds of SRAM devices were selected for azimuthal effects testing. The first kind is upset hardened by DICE [10], which is immune to single node charge collection and the sensitive node pairs must be simultaneously struck for an upset to occur [13]. The other kind is a military-level SRAM device from the Integrated Device Technology (IDT) company, which can be very sensitive to MBU [16–18] due to the layout of the memory cells. Details regarding the DUTs are reported in Table 1. The DICE SRAMs are in a thin quad flat package (TQFP) and the MBU-sensitive SRAMs are in a ceramic dual in-line package (DIP). All the test devices were de-lidded before heavy-ion exposure. IDT SRAMs contain a polyimide layer of about 60 μ m on the top of the die, which was considered in the calculation of ion energy, range, and LET.

B. Radiation source

Heavy-ion irradiations were conducted at the Heavy Ion Research Facility in Lanzhou (HIRFL), using Argon (Ar), Krypton (Kr), and Bismuth (Bi) ions with an initial energy of 25, 25 and 9.5 MeV/u, respectively. Details regarding the beam characteristics under normal incidences are presented in Table 2. The ^{209}Bi beam experiments were conducted in the vacuum chamber, while the ^{40}Ar and ^{84}Kr beam irradiations were performed in air with heavy-ions passing through a vacuum/air transition foil. A flux detector was placed in the beam line before the DUTs to monitor the real-time beam flux. The ion linear energy transfer (LET) in the DUTs was conveniently adjusted by either inserting energy degraders into the beam line (such as aluminum foils) or using angled ion strikes, i.e., the effective LET method [3]. For the angled ion

TABLE 2. Beam characteristics for experiments performed at HIRFL

Ion species	Initial Energy (MeV/u)	Energy at die surface (MeV/u)	Range (μ m)	LET (MeV cm ² /mg)
^{40}Ar	25	14.9	228.1	7.6
		10.6	139.9	9.5
		5.1	56	13.6
^{84}Kr	25	12.6	138.7	28.1
		5.7	58.8	37.4
^{209}Bi	9.5	8.8	94.6	92.6
		4.3	52.6	99.95

strikes, the effective LET was increased by a factor of $1/\cos \theta$, which can be expressed by the formula

$$\text{LET}_{\text{eff}} = \text{LET}_0 / \cos \theta, \quad (1)$$

where LET_{eff} is the effective LET of tilted ions incident at an angle of θ from the normal to the surface plane of the device and LET_0 is the initial ion LET at normal incidence.

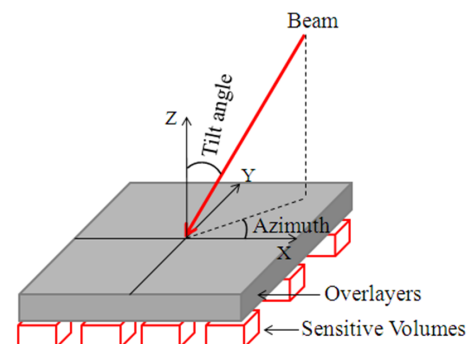


Fig. 1. (Color online) Schematic diagram of the beam direction. For clarity, the DUT is represented by sensitive volumes covered by overlayers and the substrate is not depicted.

The test boards were mounted on a four-dimension-movement platform, which allows for convenient device rotations. As shown in Fig. 1, the beam direction is defined by a tilt angle, θ , and azimuth, φ . Tilt angle controls the angle from the normal to surface plane of the device, i.e. from the positive Z -axis. Azimuth controls the angle from the projection of the incoming beam on the surface plane to the positive X -axis. The maximum tilt angle was performed under different azimuths, as long as the die would not be shadowed by the surrounding package material (which is not depicted in Fig. 1). The upset data was obtained and compared as the effective LET, i.e. the tilt angle of incident ions is the

same. During the experiments, other factors, such as beam flux, temperature, preset patterns of test devices, mode of the test system, etc., are kept constant.

C. Test systems and MBU identification

Tests were performed in a dynamic mode with a checker-board pattern input at room temperature. The memories were continuously scanned by a field programmable gate array (FPGA)-based tester. Once one bit-error was detected, several steps were performed automatically by the tester: (i) reading the erroneous bit again for confirmation; (ii) recording the bit-error information including error address, error data, and time interval of the previous error; (iii) correcting the erroneous bit; and (iv) reading the bit again to confirm the correction. The steps are finished in less than 2 μs (depending on the preset access time), then the scan process will continue at the next logical address. More than 100 bit-errors were accumulated under each test condition, in order to obtain good statistics. SEU cross sections were calculated by

$$\sigma = N_{\text{bit-error}} / (F \cdot N_b \cdot \cos \theta), \quad (2)$$

where $N_{\text{bit-error}}$ is the number of detected bit-errors, F is the beam fluence with a unit of ions/cm², and N_b denotes the device capacity. The device current was also monitored for protecting the devices burnout from a single event latchup (SEL). Once the current exceeds the preset threshold value, the power supply will be shut down automatically and the device will be reset.

For MBU identification, the recorded logical error addresses of bit-errors were converted to physical addresses based on the memory bit map [16]. One error cluster is treated as a MBU based on the following rules: (i) the errors are physically adjacent; (ii) the error data are the same due to the interleaving architecture of the test devices; and (iii) the time intervals are less than the loop period to make sure that the errors in the cluster were detected in the same loop. A few special cases, which could not be identified by those rules, were judged carefully during the identification process. Validity of those identification rules can be estimated as follows. The predominant failure mode is double adjacent bit-flips caused by two ions within the same scanning loop, whose probability can be calculated as follows:

$$P = \frac{8}{N_b} (T_{\text{loop}} R)^2, \quad (3)$$

where T_{loop} is the time of a scanning loop and R is the bit-error rate (errors/s) while irradiating, which can be controlled by the beam flux. For instance, with $N_b = 262\,144$ bits, a $T_{\text{loop}} = 6.6$ ms and $R = 10$ errors/s. Then, the failure probability equals 1.3×10^{-7} per loop. In fact, for the $\sim 10\,000$ bit-errors accumulated during the total SEU testing, there is only $\sim 2\%$ of probability that an erroneous judgment happened. Low beam flux and high scanning speed are necessary to make the identification rules valid. The MBU patterns under different azimuths were also summarized for comparison.

III. EXPERIMENTAL RESULTS AND ANALYSIS

The experimental results are presented below in the following order. First, SEU cross sections of DICE SRAMs and MBU-sensitive SRAMs under different ion azimuths, but same tilt angles, are measured and compared to probe the azimuthal dependence of single event sensitivity. Then, based on the bit-error information recorded by the test system, all types of MBUs, including double-bit upset (DBU), TBU, and QBU, were identified using the previous judgment rules. The ratios and patterns of those MBU types under different tilt angles and azimuths are shown for comparison.

A. SEU cross section

SEU cross sections of DICE-4Mb and DICE-8Mb SRAMs under normal and tilted incidence are shown in Fig. 2. Depending on the test devices, a discrepancy from 24.5% to 50% is shown between two perpendicular azimuths ($A0^\circ$ and $A90^\circ$) at the same tilt angle of 30° for ^{84}Kr ions. While the ^{209}Bi ions with a tilt angle of 30° show no clear difference in the SEU cross section between two reverse azimuths ($A0^\circ$ and $A180^\circ$). The large decrement of SEU cross sections at a tilt angle of 45° and an azimuth of 180° is attributed to the shadowed die by the surrounding package material. As a consequence, only part of SVs in the memory were exposed to irradiation, which should be paid special attention to during angular measurement of device sensitivity.

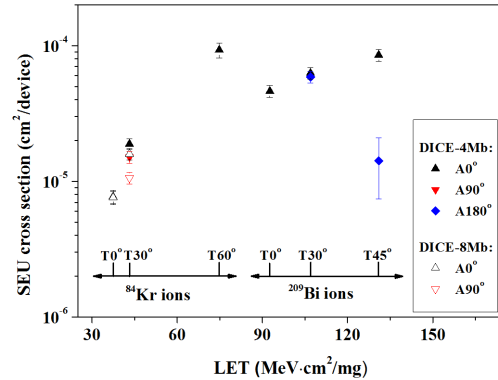


Fig. 2. (Color online) SEU cross sections of DICE-4 Mb and 8 Mb SRAM devices are plotted as a function of effective LET. The ^{84}Kr and ^{209}Bi ions were used to irradiate the devices. Under tilt angle of 30° of ^{84}Kr ions, azimuths of 0° and 90° were performed and compared. Under tilt angles of 30° and 45° of ^{209}Bi ions, azimuths of 0° and 180° were performed and compared.

Note that, at a LET value of $92.6 \text{ MeV cm}^2/\text{mg}$, the SEU cross section of DICE-4Mb SRAM under normal incidence equals $4.61 \times 10^{-5} \text{ cm}^2/\text{device}$, i.e., $1.1 \times 10^{-11} \text{ cm}^2/\text{bit}$ (treated as the plateau cross section here), which corresponds to a surface area of SV in a memory cell of about $0.0011 \mu\text{m}^2$

in the RPP model. This result can be very misleading during on-orbit error rate prediction of this RHBD-SRAM, which is built with $0.18\ \mu\text{m}$ CMOS technology. If the depth of SV is routinely set as $1\ \mu\text{m}$ (as in the CRÈME [6] or Space Radiation software [19]), this will create a long RPP with an inappropriate width(length)/depth ratio, resulting in an incorrect on-orbit error rate prediction. Moreover, the SEU cross section exhibits significant dependence on the tilt angle. The SEU cross section under a tilt angle of 60° for ^{84}Kr ions is more than one order of magnitude higher than that under normal incidence. Inverse-cosine law in the effective LET method [1] does not apply in this kind of design because the SEU cross section under a tilt incidence of 60° for ^{84}Kr ions (with an effective LET of about $75\ \text{MeV cm}^2/\text{mg}$) is one time larger than that under normal incidence for ^{209}Bi ions (with an LET of about $92.6\ \text{MeV cm}^2/\text{mg}$). Additionally, the SEU cross section continues to increase quickly, even in the effective LET range of 92.6 to $131\ \text{MeV cm}^2/\text{mg}$. One time increment was observed as the tilt angle changed from 0° to 45° .

The underlying reasons for the azimuthal dependence or independence of SEU cross section on DICE-SRAM devices lie in the device layout. A simple schematic of the DICE structure is shown in Fig. 3. As mentioned previously, the DICE topology requires a charge collection at two sensitive volumes in a memory cell for an upset to occur. Thus, the main mechanism for triggering a SEU is charge sharing, which results from the diffusion process and parasitic bipolar conduction [20], given that the incident ion cannot directly strike the two sensitive nodes simultaneously. As a consequence, the average physical distance between the two sensitive volumes along different axes, which affects the preference of the diffusion process, is a key parameter in determining the SEU response under different azimuths. The inherent anisotropic layout of RHBD structures leads to the azimuthal dependence of SEU cross sections. Similarly, due to the symmetrical distribution of sensitive nodes along the X-axis, no azimuthal dependence was observed between the azimuths of 0° and 180° .

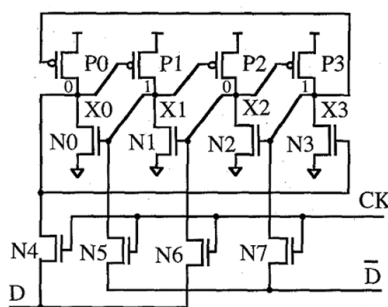


Fig. 3. The DICE memory cell.

The SEU cross sections of IDT-256kb and IDT-64kb SRAMs under normal and tilted incidence are shown in Fig. 4. Three azimuths ($A0^\circ$, $A45^\circ$ and $A90^\circ$) at tilt angles of 30° and 45° for ^{84}Kr ions were performed, but no clear azimuthal dependence was observed for both IDT SRAM de-

vices. The SEU cross section also exhibits weak dependence on the tilt angle. Those results are attributed to the fact that the SEU cross section tends to plateau in the LET region of ^{84}Kr ions and will be further discussed in the next section. Note that the SEU cross section in Fig. 4 is calculated by Eq. (2), which counts a MBU as several errors. If we count a MBU as one error, the plateau cross section of the IDT-256kb SRAM is about $1.6 \times 10^{-7}\ \text{cm}^2/\text{bit}$, corresponding to a surface area of SV in a memory cell of about $16\ \mu\text{m}^2$ in the RPP model. Unlike the DICE-SRAM discussed previously, this value fits with the reverse-engineering results shown in Fig. 5, which also supports the validity of our test results.

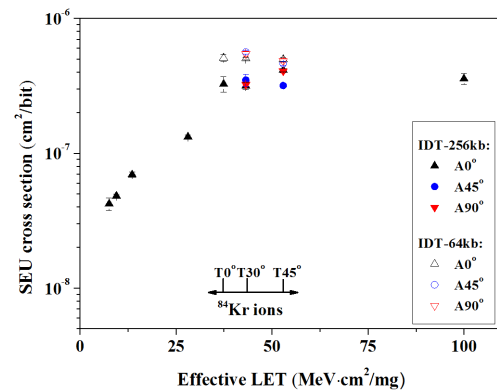


Fig. 4. (Color online) The DICE memory cell. SEU cross sections of IDT-256kb and 64kb SRAM devices are plotted as a function of effective LET. The ^{40}Ar and ^{209}Bi ions were used to irradiate the devices under normal incidence. Under tilt angles of 30° and 45° of ^{84}Kr ions, azimuths of 0° , 45° and 90° were performed and compared.

B. MBU ratios and patterns

For the DICE-SRAM devices, due to the hardened design, only a few DBUs were detected under the largest tilt angle. Thus, no enough data was acquired to investigate the azimuthal dependence on the MBU ratio. While for the IDT-256kb SRAM, as studied by Koga *et al.* [16] and our previous work [17, 18], MBU can be easily triggered under tilted incidence. Moreover, we found that under normal incidence, MBU accounted for more than half of all the bit-errors at an LET value of $37.4\ \text{MeV cm}^2/\text{mg}$, with increasing probability as tilt angle increased. However, the increment of MBU ratio as tilt angle changed from 0° to 45° was less than 10% and no clear difference was observed between MBU ratios under different azimuths and the same tilt angle, which explained the weak dependence of SEU cross sections on the tilt angle and azimuth (note that the SEU cross section here treated a MBU as several errors).

To analyze the MBU characteristics in more detail, MBU patterns under different azimuths are further investigated. Here, MBU pattern means the physical arrangement of the

TABLE 3. Cumulative DBU patterns induced by ^{84}Kr ions at normal incidence and at tilt angle of 30° and 45° under three azimuths in IDT-256kb SRAMs

Tilt angle	Azimuth	DBU patterns				
0°	0°	107	63	24	0	1
	30°	126	58	15	0	0
	45°	129	82	29	0	1
30°	0°	97	65	23	0	1
	45°	170	52	15	0	1
	90°	143	57	30	0	0
45°	0°	97	98	16	1	1
	30°					
	45°					

flipped-bits in a MBU. DBU patterns induced by ions at normal and tilted incidences under three azimuths are reported in Table 3. For the normally incident ions, the majority of DBU events involved two adjacent cells along the X -axis, followed by the occurrence of two adjacent cells along the Y -axis and two cells in the diagonal. The underlying reasons are discussed as follows. As shown in Fig. 5, sensitive regions of adjacent cells are periodically separated by the bitline/bitline bar (BL/BLB) contacts along the Y -axis direction, causing anisotropic distribution of sensitive volumes in the device layout. Thus, charges created by normally incident ions in the p-well can more easily diffuse to be shared by horizontally adjacent cells, due to the shorter inter-cell distance, leading to more DBUs along the X -axis.

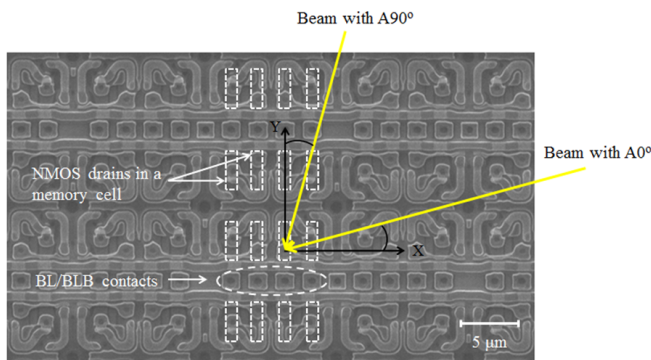


Fig. 5. (Color online) Scanning Electron Microscope (SEM) picture at POLY of IDT-256kb SRAM device after reverse engineering. Two NMOS drains in the 4-transistor, polysilicon resistor load SRAM cell are marked in the figure. One of them is considered as the SEU sensitive region, depending on the storage state of the memory cell.

For the tilted incidence, DBU patterns induced by ions under three azimuths are listed in Table 3. Here, we define a parameter, R , which equals the amount of along- X -axis DBUs divided by the amount of along- Y -axis DBUs, as a useful parameter for comparison. Note that R varies dramatically from 3.3 to 1 as the azimuth of incident ions changes from 0° to 90° (with tilt angle of 45°). Additionally, tilted ions at the diagonal incidence, i.e., under an azimuth of 45° , in-

duce about twice the amount of diagonal DBUs than the other two azimuths with a tilt angle of either 30° or 45° . Those results suggest that tilted ion-induced MBU patterns are ion trajectory-oriented. As illustrated in Fig. 5, although the tilt angle is the same, the direction of ion trajectory among the SVs is different for beam with $A0^\circ$ or $A90^\circ$, inducing preferable DBU patterns along the incident direction. To conclude, the beam direction relative to the layout of the device strongly impacts the DBU patterns, which are also affected by the spatial layout of SVs.

Due to smaller dimensions, compared to other patterns, L-shaped and square-shaped configurations are the predominant patterns of TBU and QBU, respectively (see Table 4 and Table 5), regardless of the beam direction. Similar results about predominant MBU patterns induced by protons with different energies were shown and discussed in Ref. [21]. Trajectory-oriented patterns are identified again in the non-predominant QBU patterns, although fewer events were observed.

IV. IMPLICATIONS FOR HARDNESS ASSURANCE TESTING

Previous experimental results pose great challenges to the applicability/accuracy of the RPP/IRPP model in RHBD devices. As stated before, one inherent assumption of the RPP model is that the charges resulting into an upset are collected in a single volume. Based on that, several important parameters, such as surface sensitive area and critical charge, can be extracted from the earth-based testing results for on-orbit error rate predictions. However, for RHBD devices (such as DICE, TMR, or ADE), the RPP/IRPP model may fail or underestimate the on-orbit error rates if only normally incident ions are used for measurements in the earth-based testing. Those hardening approaches are inherently sensitive to tilted incidence and azimuthal testing. Angular and azimuthal dependence on SEU cross sections in DICE circuits should be considered in the hardness assurance testing and error rate prediction method. To avoid underestimation of the device sensitivity, azimuthal testing should be conducted to find the worst case response, especially in devices with an anisotropic layout.

As technology downscales, MBUs are becoming increasingly important, due to reduced cell distance, reduced cell sensitivity, and reduced cell dimensions. MBUs can significantly contribute to the error rates. Traditional RPP/IRPP models should be promoted to take this effect into consideration, especially for advanced MBU-sensitive memories. The inner mechanisms that should be considered includes charge drifting, diffusion, parasitic bipolar amplification, and also ion track effects, which is particularly important in nanometric devices since that single ion track can be large enough to cover several SVs. Angular and azimuthal dependence on MBU response in the previous results also suggest the necessity of complete tilted ion strikes during heavy-ion accelerator tests in MBU-sensitive devices, which is also motivated by the fact that space particles strike the devices from all directions.

TABLE 4. Cumulative TBU patterns induced by ^{84}Kr ions at normal incidence and at tilt angle of 30° and 45° under three azimuths



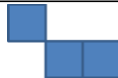







Tilt angle	Azimuth	TBU patterns					others
							
0°	0°	70	0	0	0	0	0
30°	0°	77	2	0	0	1	0
	45°	83	3	1	0	0	0
45°	90°	94	1	0	0	0	0
	0°	89	5	1	0	0	0
	45°	102	4	0	1	0	0
	90°	114	0	0	0	0	0

TABLE 5. Cumulative QBU patterns induced by ^{84}Kr ions at normal incidence and at tilt angle of 30° and 45° under three azimuths

Tilt angle	Azimuth	QBU patterns					others
							
0°	0°	7	0	0	0	0	0
30°	0°	1	0	0	0	0	0
	45°	3	0	0	0	0	0
45°	90°	4	0	0	0	0	0
	0°	7	3	1	0	0	0
	45°	4	1	1	0	0	1
	90°	6	0	0	4	2	2

V. CONCLUSION

Heavy-ion experiment results show that beam direction relative to the layout of test device can be of significant importance in SEE responses of anisotropic SRAM devices. Direct comparisons between three beam azimuths are performed with ions incident at the same tilt angles, i.e., same effective LET. The strong impact of ion azimuth on the SEU data and MBU patterns of DICE and MBU-sensitive SRAM devices are observed in this work. In the DICE-SRAM devices, a discrepancy from 24.5% to 50% in the SEU cross section is shown between two perpendicular azimuths at the same tilt angle of 30° . The primary reason lies in the anisotropic distribution of SVs in the DICE structure. Moreover, the SEU cross section exhibits significant dependence on the tilt angle. Inverse-cosine law in the effective LET method does not apply in this kind of design.

Due to the BL/BLB contact isolations of SVs along the Y-axis, the majority of DBU events induced by normally

incident ions involve two adjacent cells along the X-axis. Ion trajectory-oriented MBU patterns are identified, although the predominant TBU and QBU patterns are the same (L-shaped and square-shaped configurations, respectively) under different azimuths. MBU patterns are determined by both the device layout and the beam direction.

Those results reveal azimuthal and tilted dependence of SEU data and MBU patterns in RHBD and MBU-sensitive SRAMs, which pose great challenges to the validity of the traditional RPP/IRPP model in those devices. In earth-based testing, azimuthal effects should be considered to find the worst case response, especially in devices with an anisotropic layout.

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[1] Dodd P E, Shaneyfelt M R, Schwank J R, *et al.* Current and future challenges in radiation effects on CMOS electronics. IEEE T Nucl Sci, 2010, **57**: 1747–1763. DOI: 10.1109/TNS.2010.2042613

[2] Tong T, Wang X H, Zhang Z G, *et al.* Effectiveness and failure modes of error correcting code in industrial 65 nm CMOS SRAMs exposed to heavy ions. Nucl Sci Tech, 2014, **25**: 010405. DOI: 10.13538/j.1001-8042/nst.25.010405

- [3] Raine M, Gaillardin M, Paillet P, *et al.* Angular dependence of SOI transistor response to heavy ion irradiation. *IEEE T Nucl Sci*, 2010, **57**: 3219–3227. DOI: [10.1109/TNS.2010.2077309](https://doi.org/10.1109/TNS.2010.2077309)
- [4] Pickel J C and Blandford J T. Cosmic-ray-induced errors in MOS devices. *IEEE T Nucl Sci*, 1980, **27**: 1006–1015. DOI: [10.1109/TNS.1980.4330967](https://doi.org/10.1109/TNS.1980.4330967)
- [5] Petersen E, Langworthy J and Diehl S. Suggested single event upset figure of merit. *IEEE T Nucl Sci*, 1983, **30**: 4533–4539. DOI: [10.1109/TNS.1983.4333166](https://doi.org/10.1109/TNS.1983.4333166)
- [6] CRÈME site. <https://creme.isde.vanderbilt.edu/>
- [7] EIA/JESD57: Test procedure for the measurement of single-event effects in semiconductor devices from heavy ion irradiation, 1996.
- [8] Petersen E L. Single event analysis and prediction. *IEEE Nuclear and Space Radiation Effects Conference Short Course*. Tucson, A Z, July, 2008.
- [9] Weller R A, Mendenhall M H, Reed R A, *et al.* Monte Carlo simulation of single event effects. *IEEE T Nucl Sci*, 2010, **57**: 1726–1746. DOI: [10.1109/TNS.2010.2044807](https://doi.org/10.1109/TNS.2010.2044807)
- [10] Calin T, Nicolaidis M and Velazco R. Upset hardened memory design for submicron CMOS technology. *IEEE T Nucl Sci*, 1996, **43**: 2874–2878. DOI: [10.1109/23.556880](https://doi.org/10.1109/23.556880)
- [11] Liu M S, Liu H Y, Brewster N, *et al.* Limiting upset cross sections of SEU hardened SOI SRAMs. *IEEE T Nucl Sci*, 2006, **53**: 3487–3493. DOI: [10.1109/TNS.2006.886216](https://doi.org/10.1109/TNS.2006.886216)
- [12] Baze M P, Hughlock B, Wert J, *et al.* Angular dependence of single event sensitivity in hardened flip/flop designs. *IEEE T Nucl Sci*, 2008, **55**: 3295–3301. DOI: [10.1109/TNS.2008.2009115](https://doi.org/10.1109/TNS.2008.2009115)
- [13] Warren K M, Sierawski B D, Reed R A, *et al.* Monte-Carlo based on-orbit single event upset rate prediction for a radiation hardened by design latch. *IEEE T Nucl Sci*, 2007, **54**: 2419–2425. DOI: [10.1109/TNS.2007.907678](https://doi.org/10.1109/TNS.2007.907678)
- [14] Amusan O A, Massengill L W, Baze M P, *et al.* Directional sensitivity of single event upsets in 90 nm CMOS due to charge sharing. *IEEE T Nucl Sci*, 2007, **54**: 2584–2589. DOI: [10.1109/TNS.2007.907989](https://doi.org/10.1109/TNS.2007.907989)
- [15] Tipton A D, Pellish J A, Hutson J M, *et al.* Device-orientation effects on multiple-bit upset in 65 nm SRAMs. *IEEE T Nucl Sci*, 2008, **55**: 2880–2885. DOI: [10.1109/TNS.2008.2006503](https://doi.org/10.1109/TNS.2008.2006503)
- [16] Koga R, Crawford K B, Grant P B, *et al.* Single ion induced multiple-bit upset in IDT 256K SRAMs. *Second European Conference on Radiation and its Effects on Components and Systems*. St. Malo, Sep.13–16, 1993, 485–489. DOI: [10.1109/RADECS.1993.316526](https://doi.org/10.1109/RADECS.1993.316526)
- [17] Zhang Z G, Liu J, Hou M D, *et al.* Angular dependence of multiple-bit upset response in static random access memories under heavy ion irradiation. *Chinese Phys B*, 2013, **22**: 086102. DOI: [10.1088/1674-1056/22/8/086102](https://doi.org/10.1088/1674-1056/22/8/086102)
- [18] Zhang Q X, Hou M D, Liu J, *et al.* The impact of incident angle on multiple-bit upset in SRAMs. *Nucl Instrum Meth B*, 2003, **209**: 367–370. DOI: [10.1016/S0168-583X\(02\)02026-8](https://doi.org/10.1016/S0168-583X(02)02026-8)
- [19] Space radiation. <http://www.spacerad.com/>
- [20] Olson B D, Ball D R, Warren K M, *et al.* Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design. *IEEE T Nucl Sci*, 2005, **52**: 2132–2136. DOI: [10.1109/TNS.2005.860684](https://doi.org/10.1109/TNS.2005.860684)
- [21] Radaelli D, Puchner H, Wong S, *et al.* Investigation of multi-bit upsets in a 150 nm technology SRAM device. *IEEE T Nucl Sci*, 2005, **52**: 2433–2437. DOI: [10.1109/TNS.2005.860675](https://doi.org/10.1109/TNS.2005.860675)